a gate electrode provided adjacent to said channel formation region with a gate insulating film interposed therebetween.

48. (Amended) The device of claim 47 wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

53. (Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, and a second resinous substrate opposed to said first resinous substrate;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface; and

a thin-film transistor provided on said planarized surface of said resinous layer;

an interlayer insulating layer comprising a resinous material provided over said thin-film transistor; and

at least one pixel electrode provided on said interlayer insulating layer,

wherein said thin-film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region between said source region and said drain region; and

a gate electrode provided over said channel formation region with a gate insulating film interposed therebetween.

54. (Amended) The device of claim 53 wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

59. (Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, and a second resinous substrate opposed to said first resinous substrate, wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface;

a thin film transistor provided on said planarized surface of said resinous layer; and

an interlayer insulating layer comprising resinous material provided over said thin film transistor,

wherein said thin film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film interposed therebetween.

64. (Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, and a second resinous substrate opposed to said first resinous substrate, wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface;

a thin film transistor provided on said planarized surface of said resinous layer; and

an interlayer insulating layer comprising resinous material provided over said thin film transistor,

wherein said thin film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided over said channel formation region with a gate insulating film interposed therebetween.

69. (Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, and a second resinous substrate opposed to said first resinous substrate, wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface;

a thin film transistor provided on said planarized surface of said resinous layer; and

an interlayer insulating layer comprising resinous material provided over said thin film transistor,

at least one pixel electrode provided on said interlayer insulating layer,

wherein said thin film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided over said channel formation region with a gate insulating film interposed therebetween.